IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

First Named Inventor: FUKUDA, KEIKO | Art Unit: 4125

Appln. No.: 10/584,395 | Examiner: COLE, BRANDON S.

Filed: June 23, 2006 | Confirmation No.: 9000

For: VOLTAGE GENERATION CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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INFORMATION DISCLOSURE STATEMENT
AND STATEMENT UNDER 37 C.F.R. § 1.97(e)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the documents listed on the attached Form PTO/SB/08A are hereby cited.

Document 2 was cited in a counterpart Chinese application (copy of Chinese Office Action and English translation attached). Document 1 is a U.S. Counterpart of Document 2. It should be noted that the other document listed in the Office Action is already of record in the instant application.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10578) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account.

STATEMENT UNDER 37 C.F.R. § 1.97(e)

The undersigned hereby states that no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Respectfully submitted,

Date: October 6, 2008

By: ___/Patrick L. Miller/___
Mitchell W. Shapiro
Reg. No. 31,568

Patrick L. Miller
Reg. No. 57,502

Miles & Stockbridge, P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

MWS:ecr